Low-Spur Numerically Controlled Oscillator Using Taylor Series Approximation

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1. Introduction

The Numerically Controlled Oscillator (NCO) synchronously and sequentially generates digital samples of the sine wave. The name "numerically controlled" means that the rate at which sine wave samples appear at the output of the NCO and the number of sine samples per period can be set by a microcomputer or a microcontroller. NCO is the main building block of the frequency- or waveform synthesizers. Frequency synthesizers play an important role in modern communication and instrumentation equipment where they are used to generate a sinusoidal or digital signal with required frequency [1]. Waveform synthesizers are used to synthesize sinusoidal voltages with very accurate effective value [2], [3], [4] or waveforms which shape can be defined by the user (arbitrary waveform synthesizers) [5].

2. Short classification of NCOs

There are generally three types of NCOs:

1. Based on a digital counter addressing a read-only memory (ROM). The ROM works as a look-up table (LUT), containing the set of digital sine samples. The address value of the ROM represents the phase of the sine function. This address is generated by a digital counter. The rate at which the digital sine samples appear at the output of the NCO is determined by the frequency clocking the counter. The number N of samples per period of the generated sinusoid is fixed. However, a single ROM may contain several sets of digital samples of the sinusoid, each with different number of samples per period. The required set is chosen by a few most significant bits (MSB) of the ROM address bus. The look-up table based NCOs are used mainly in Digitally Synthesized Sources (DSS), used for generation of standard AC voltages [2].
2. Based on a computer calculating sine samples in real time. The computer can be implemented using a Digital Signal Processor (DSP) or a Field Programmable Gate Array (FPGA) performing the sine computation using an appropriate algorithm, like CORDIC [6]. This kind of NCOs, especially those equipped with a DSP, are used in ultra-low distortion generators used for testing audio equipment [7].
3. Based on the Direct Digital Synthesizer (DDS) principle, which will be described in the next paragraph. In the DDS the digital counter addressing the LUT is replaced with registered adder forming so called phase accumulator. The DDSs are mainly used as frequency synthesizers as they able to set the frequency of the generated signal with very high resolution. Moreover, the frequency change takes a very short time, making DDS frequency synthesizers usable in applications requiring frequency hopping. Actually, the NCOs based on the DDS principle seem to be the most popular, mainly because of their wide usage in communication equipment.

3. NCO of the conventional DDS

The general block diagram of the DDS is shown in Fig. 1 [1], [8], [9]. It contains few main blocks: phase accumulator, phase-to-amplitude converter, digital-to-analog converter (DAC) and low-pass filter (LPF). The phase accumulator and the phase-to-amplitude converter form the NCO. The phase accumulator is composed of an adder and a phase register. The actual value at the output of the phase accumulator is the sum of the phase increment value T and the previous value $\varphi(n)$ stored in the phase register. The phase accumulator has limited capacity and overflows when the value at its output is greater than 2^A-1, where A is number of bits of the phase accumulator. The rate at which the accumulator overflows determines the output frequency f_o generated by the DDS which is equal to:

$$f_o = \frac{T}{2^A} f_s, \tag{1}$$

where f_s is the clock frequency and T is the frequency tuning word representing the phase increment by which the phase accumulator is increased with each clock. The output of the phase accumulator is always an integer value. The phase-to-amplitude converter is

usually the Read Only Memory (ROM) which stores values of the properly scaled and coded sine samples. This memory is called also the look-up table.

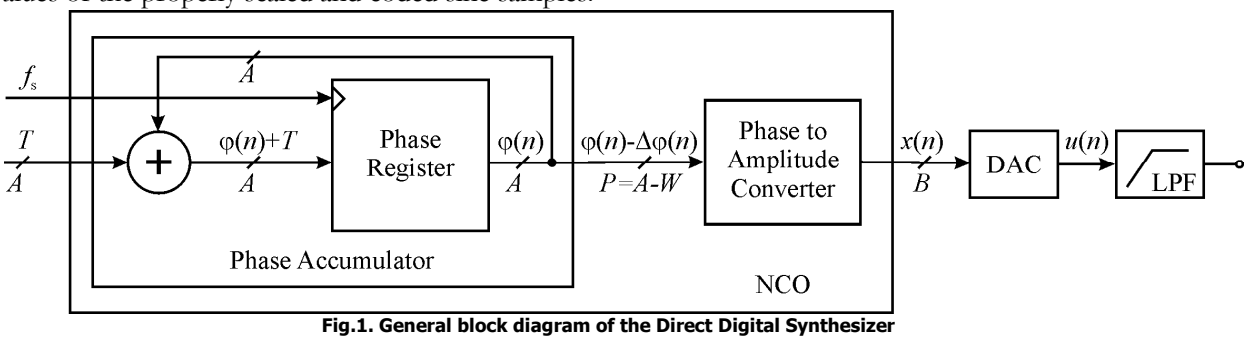

Fig.1. General block diagram of the Direct Digital Synthesizer

The address bus of the LUT is driven by the all or by the several the most significant (MSB) bits of the phase accumulator. The data bus of the LUT drives the digital input of the DAC. In the ideal case, when all bits of the output bus of the phase accumulator are used to address the LUT and the digital sine samples stored in the LUT have infinite precision, the output value at the phase-to-amplitude converter may be expressed by:

$$x(n) = \sin\left(2\pi \frac{\varphi(n)}{2^A}\right), \tag{2}$$

where $\varphi(n)$ is the value of the word at the phase register after n-th clock tick, equals:

$$\varphi(n) = \langle n \cdot T \rangle_{2^A}, \tag{3}$$

where $\langle x \rangle_y$ represents taking the integer residue of a number x modulo y.

4. Sources of spurs in DDS

The number A of phase accumulator bits of a DDS is usually between 24 and 64. It would require irrationally high storage capacity ROM to use the full width of the phase accumulator word and sine digital samples with, for example, 16 bit precision. To reduce the memory size, the phase accumulator output word is usually truncated, i.e. the W least significant bits (LSB) of the phase accumulator output bus are not fed to the LUT address bus [10], [12]. The truncation of the phase accumulator word produces unwanted harmonics in the frequency spectrum of the signal generated by the NCO. These unwanted harmonics are called spurs. To further reduce the size of the LUT, the sine wave stored in ROM is compressed [9]. The compression of the sine wave stored in LUT is the second source of the spurs in the signal generated by the NCO.

5. Spurs due to truncation of the phase accumulator word

Considering the truncation effect only (no compression of data stored in LUT), the value of the n-th sample is given by the equation:

$$x(n) = \sin\left(2\pi \frac{\varphi(n) - \Delta x(n)}{2^A}\right), \tag{4}$$

where $\Delta x(n)$ is the phase truncation error. Equation (4) reveals an unwanted phase modulation, which is the source of additional unwanted spectral components in the output signal, called spurs. The number n_h of spurs in the first Nyquist zone (0 to $f_{CLK}/2$) of the frequency spectrum is equal to [11]:

$$n_h = \frac{2^W}{\mathrm{GCD}(T, 2^W)} - 1, \tag{5}$$

where GCD is the Greatest Common Divisor of T and 2^W. The amplitude ζ_{max} of the strongest unwanted harmonic is equal to [10]:

$$\zeta_{max} = 2^{-P} \frac{\pi \cdot \mathrm{GCD}(T, 2^W)}{\sin \pi \cdot 2^{-C} \mathrm{GCD}(T, 2^W)}, \tag{6}$$

where P is the number of bits in the phase-to-amplitude converter input bus ($P = A - W$). The strongest spurs occur, when value of the frequency tuning word satisfies the condition [1]:

$$\mathrm{GCD}(T, 2^W) = 2^{W-1}. \tag{7}$$

If $W > 4$ then the maximum spur level (expressed in dBc) may be estimated from simple equation:

$$\zeta_{max} \approx -6.02 \cdot P. \tag{8}$$

The next problem is that the subsequent periods of the sinusoidal signal generated by the DDS-type of NCO generally do not consist of the same digital sine samples. Analysis shows that the same set of sine samples in each subsequent period occurs, when there is no truncation, i.e. for values of T satisfying the condition [1]:

$$\mathrm{GCD}(T, 2^W) = 2^W. \tag{9}$$

For the other values of T the sequence of samples repeats after a certain number of samples called Grand Repetition Rate (*GRR*). This number may be calculated from the equation [1]:

$$GRR = \frac{2^A}{\mathrm{GCD}(T, 2^A)}. \quad (10)$$

The *GRR* may be substantially high for high resolution NCOs where the number of bits *A* is usually 48 or greater. This effect may be disturbing in some applications, like [2], [3], [4], [13]. Moreover, the long *GRR* suggests that there are unwanted low-frequency subharmonics in the generated signal.

6. Reduction of spurs

Several techniques have been developed to reduce the spurs caused by the truncation of the phase word effect. One of the simplest methods is to force *T* to be always odd [10]. For $C > 4$ it reduces truncation spurs by approximately 3.9 dB, but the penalty is halving the resolution of the frequency resolution setting of the synthesizer with so modified NCO. An alternative method is Taylor series correction [9], [12] or random phasing correction [14]. The new method of reduction, based on the Taylor-series approach is presented in the next paragraph.

7. The new approach

As it was mentioned, the conventional DDS-based NCO is generally unable to generate signal with the same set of digital sine samples in the each subsequent period. To avoid that problem an NCO with a special coprocessor calculating sine samples was elaborated and will be implemented in the modern high-speed FPGA. The NCO will contain the same basic building blocks of the conventional DDS like adder and phase register, but instead of the LUT, the built-in special coprocessor will calculate each sine sample in the real time. So far, coprocessors exist which are calculating sine and cosine waveforms using the iterative CORDIC algorithm [6]. Unfortunately the CORDIC algorithm needs too many iterations to complete calculation with accuracy needed for low-spur NCOs. Therefore instead of CORDIC, a new algorithm will be used, which is able to calculate the value of the sine sample with required accuracy in shorter time. The simplified architecture of the new NCO is shown in Fig. 2. It contains two digital inputs: with one of them user defines the number *N* of the samples per period. To second input the clocking signal is applied. Output frequency of the signal generated by this NCO sine wave is equal to:

$$f_o = f_s / N. \quad (6)$$

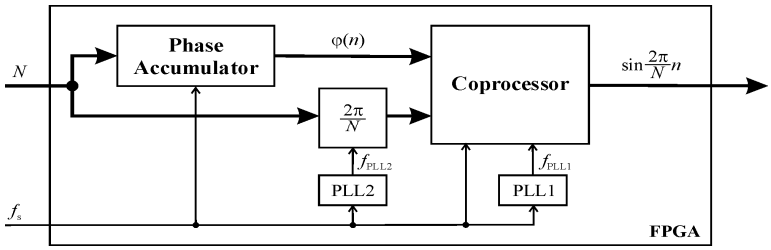

Fig.2. General block diagram of the proposed NCO

In each cycle of f_s coprocessor calculates new value of the next sample. The values of the sine sample are calculated with a special coprocessor clocked with frequency f_{PLL1}. This frequency is achieved by multiplying the f_s with the internal PLL circuit which is a part of the Digital Clock Manager (DCM) built in Xilinx FPGA. In this particular case PLL1 works as frequency multiplier. Ratio of f_{PLL1} to f_s should be as small as possible, because this ratio determines the output frequency of NCO. Let's assume that this ratio is equal to 9. To achieve output frequency f_o of the NCO equal to 100 MHz, the frequency f_{PLL1} should be as high as 900 MHz. In this case it is the challenge to keep this ratio relatively small and keep high accuracy of the generated sample. The proposed NCO contains also second frequency multiplier PLL2. It is used by the second additional coprocessor, which will be used mainly for calculation of the reciprocal function 1/*N*. Actually the Goldschmidt algorithm is considered to be implemented for this purpose [15]. The main coprocessor will calculate the sine samples using a novel algorithm based on Taylor series sine approximation (to be more specific - MacLaurin series). This novel algorithm is the crucial point of the new NCO and will be presented in a future paper.

8. Preliminary results and prospects

The novel architecture has been implemented in Matlab/Simulink environment using Xilinx System Generator tool. Phase accumulator was written in VHDL. The results are shown in Fig. 3. Figure 3a shows absolute sine approximation error of 1000 sine samples per period using conventional Taylor series algorithm calculating samples in range from 0 to 2π. To achieve error shown in Fig. 3a the coprocessor needs to calculate the Taylor series up to the x^{15} term. The error for the novel NCO using the new algorithm is shown in Fig. 3b. The error shown in Fig. 3b was determined for 5000 sine samples per period using the novel algorithm running in very crude one-quarter approximation range. To achieve error shown in Fig. 3b the coprocessor had to calculate the Taylor series only

up to the x^7 term. The novel algorithm is modifiable, and errors below 10^{-11} are easy attainable. Further work will be focused on improving the speed of the algorithm and on the implementation of the NCO in a silicon device.

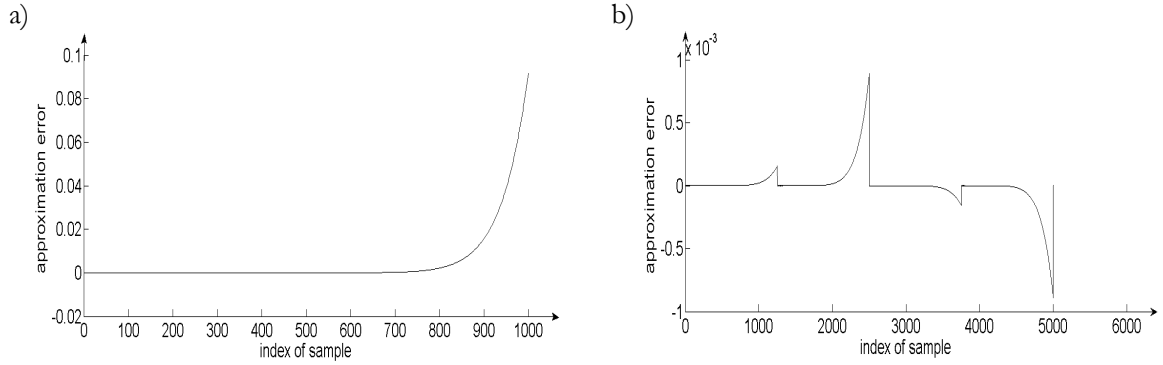

Fig. 3. Approximation error of the sinus function generated by the: a) conventional NCO with Taylor series, b) novel NCO

9. Bibliography And Authors

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