Novel Zero-Voltage and Zero-Current Switching Full-Bridge PWM Converter Using Simple Secondary Active Clamp Circuit

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Abstract
A novel zero-voltage and zero-current switching (ZVZCS) full-bridge (FB) phase shifted pulse-width modulation (PWM) converter is presented in this paper. A simple auxiliary circuit on the secondary side provides conditions for ZVZCS of insulated gate bipolar transistors (IGBT’s) on the primary side of the DC/DC converter. The turning off the MOSFET transistor located on the secondary side provides reset both secondary and primary current and thus the conditions for ZVZCS is achieved. The features, principle operation and design considerations of the converter are illustrated and verified on proposed converter.

1. Introduction
Recently, the increasing demands for high performance load converters in power electronics are present. It also places great emphasis on increasing the switching frequency for reducing size and weight of the converters. However with increasing frequency the increasing switching losses occur mainly on the switching devices such as transistors.

The MOSFETs are mainly used as switching devices in ZCZVS FB PWM converters. Even if their many advantages, for instance very short switching times, there are not suitable for high power applications.

These days, IGBTs are replacing MOSFETs for high voltage, high power applications, since IGBTs have higher voltage rating, higher power density, and lower cost compared to MOSFETs [1]. On the other hand, the use of IGBTs is significantly reduced by their frequency switching, usually limited to 20–30 kHz because of their tail current characteristic [2]. To operate IGBTs at higher switching frequencies is required to significantly reduce turn-off switching losses.

Many topologies have been developed to solve this problem [1]–[5]. This topology used auxiliary circuit on the secondary side to achieve ZCZVS and therefore to reduce the switching loss to zero. Generally the ZVS of the leading-leg switched is achieved by the similar manner as that of the ZVS FB PWM converters [3] – [4], [6] whereas ZCS of lagging-leg switches is achieved by resetting the primary current during the freewheeling period. The technical realization of auxiliary circuit which provides reset of primary current is realized in different ways. The converter proposed in [3] has simple auxiliary circuit which contains neither loss components nor active switches. Resetting of the primary current is achieved using energy of leakage inductance and clamp capacitor placed on the secondary side. The converter [2] same as converter [3] contains neither loss components nor active switches. Resetting of the primary current is achieved using transformer auxiliary winding inserted into the secondary side what makes this auxiliary circuit more complex. The converter [7] contains active switch on the secondary side. This switch is used to control the clamping circuit. The clamp switch induces switching loss due to its hard switching, and the maximum output current is limited by the capacitance of holding capacitor [3]. The blocking capacitor on the primary side of the transformer winding is used in the converter [5]. The auxiliary circuit contains active switch and transformer auxiliary winding which make this circuit considerably complex and parameter design is complicated [2].

2. Operation principle
The proposed converter Fig.1 has nine operating modes within each operating half cycle. The equivalent circuits and the corresponding operation waveforms are shown in Fig.2 and Fig.3, respectively.

The detail description of proposed converter is in [6]. This operation principle description below is abbreviated form of description in [6].
The collector current of the transistor $T_1$ turns on with ZVS at $t_0$ because only magnetizing current flows through diodes $D_1$, $D_2$. The collector current of the transistor $T_s$, which is turned on at $t_0$, too, starts to flow and the capacitor $C_C$ is discharged.

The rise of the collector current is in resonant way with the resonant frequency $\omega_{R1}$ different at no-load and short circuit in a range:

$$\sqrt{(L_0 + L_{CS}) \frac{C_0 C_C}{C_0 + C_C}} \leq \omega_{R1} \leq \sqrt{(L_0 + L_{CS}) C_C}$$

Mode2-interval ($t_0$–$t_2$): The transformer leakage inductance $L_{LP}$ reflected to the primary side causes that primary current $i_{p}$ is linearly increased with the slope $U/L_{LP}$ while the secondary voltage $u_s$ is zero as a result of commutation between output freewheeling diode $D_0$ and rectifier diode $D_3$.

Mode3-interval ($t_2$–$t_3$): The commutation between diode $D_0$ and output freewheeling diode $D_0$ is finished and the end of this interval the clamp capacitor current commutates to clamp diode $D_5$.

Mode4-interval ($t_3$–$t_4$): The energy delivered from the source to the load through transistors $T_1$ and $T_2$ which are conducting. The smoothing inductance current is a sum of the secondary current and inductance $I_{LS}$ current:

$$i_o = i_s + i_{LS}$$

Mode5-interval ($t_4$–$t_5$): The primary current increases with the slope:

$$\frac{di_p}{dt} = \frac{U - nU_0}{L_{LP} + n^2 L_0} + \frac{U}{L_{in}}$$

Where $n = \frac{N_p}{N_S}$ is power transformer turns ratio and $L_{in}$ magnetizing inductance of the power transformer.

Mode6: interval ($t_5$–$t_6$): At $t_5$ the secondary transistor $T_5$ turns off. At that time the commutation between transistor $T_5$ and clamp diode $D_5$ occurs and charging of the clamp capacitor $C_C$ starts. Afterwards the commutation between $D_C$, $D_3$ and output freewheeling diode $D_0$ starts. In the mentioned commutation path the resonance occurs and rise of the current depends on the resonant frequency $\omega_{R2}$:

$$\omega_{R2} = \sqrt{(L_0 + L_{LS}) \frac{C_0 C_C}{C_0 + C_C}}$$

Mode7- interval ($t_6$–$t_7$): Only small magnetizing current $i_m$ flows through primary winding of transformer. The output current flows trough output freewheeling diode $D_0$.

Mode8 - interval ($t_7$–$t_8$): In this interval the transistors $T_1$ and $T_2$ are turned off with ZCS. Only small magnetizing current $i_m$ is switched off by transistors $T_1$ and $T_2$. The magnetizing current charges or discharges the internal output capacitances $C_{CSS1} - C_{CSS4}$ of the IGBT transistors $T_1 - T_4$ respectively.

The minimum dead time $t_d$ for the transistors in the leg is given by:

$$t_{d_{min}} \geq t_{recon}$$

where $t_{recon}$ is minority carrier recombination time of IGBT’s due to stored charges that could not be removed at turn-off process.

Mode9 - interval ($t_8$–$t_9$): At $t_8$ the freewheeling diodes $D_3$, $D_4$ starts to lead primary current and thus conditions for the ZVS for the transistors $T_3$ and $T_4$ are set up.
3. Simulation results

A simulation model in programme Orcad was created to verify the properties of the proposed converter. The simulations were performed at input voltage $U = 300V$.

Parameters:
Transformer TR parameters:
- Turns ratio $n = 6$,
- Magnetizing inductance $L_m = 1 \text{ mH}$,
- Leakage inductance $L_{Lp} = 5 \mu\text{H}$.
Clamp circuit parameters:
- Clamp capacitor $C_C = 400 \text{ nF}$,
- Clamp inductance $L_S = 5 \mu\text{H}$.

Fig.4 shows the waveforms during turn-on and turn-off of the primary switch $T_4$. The influences of secondary active clamp circuit insure that all switching devices are switched softly. As we can see the leading-leg for transistor $T_4$ is switched softly and the switching loss is neglectable.

Fig.5 shows the secondary voltage $u_{DS}$ and collector current $i_D$ of the transistor $T_3$ (upper waveforms) in comparison with switch waveforms of voltage $u_{CE}$ and collector current $i_C$ of transistor $T_4$ (bottom waveforms). It can be seen that influence of leakage inductance $L_{LS}$ of transformer and clamp inductance $L_S$ insure that turn-on of the transistor $T_4$ is under zero-current and just as in the previous case (Fig.4) the power losses can be neglectable, too.

Fig.6 and Fig.7, respectively, show the simulation waveforms of voltage $u_S$ and collector current $i_D$ of transistor $T_3$ (upper waveforms) in comparison with primary voltage $u_p$ and current $i_p$ (bottom waveforms of Fig.6). After turned-off of secondary transistor $T_3$ only small magnetization current $i_m$ flows through the primary winding. This current charges and discharges the internal capacity of transistors $T_1$ – $T_4$, respectively, and so the condition of ZVS is achieved. Fig.7. (bottom waveforms) shows the simulation waveforms of currents flows through the clamp capacitor $C_C$, the diode $D_S$ and the clamp diode $D_C$ during cycle of the operation $T_3$.

Fig.2. Equivalent circuit for each operation mode (Note—the blue color shows components among which commutations occur).

Fig.3. Operation waveforms of the proposed converter.

Fig.4. Switch voltage $u_{CE}$ and collector current $i_C$ of transistor $T_4$. 

U_{CE}(T4)  I_C(T4)
4. Experimental results

A prototype of the proposed ZVZCS-FB-PWM converter has been built and tested to verify the principle of the operation. The coaxial transformer used has been laboratory built with turn ratio \( n = 6 \). The main inductance of the transformer is 981.5 \( \mu \)H and the primary leakage inductance is 18.5 \( \mu \)H. The prototype of the converter was supplied by 300 VDC and switching frequency of IGBT’s was 50kHz. The main parameters are summarized in Tab.1.

The voltage and current of the primary switch \( T_4 \) and the transistor \( T_s \) situated on the secondary side are shown in Fig.8. Fig.9 shows extended waveforms of the transistor \( T_s \). The value of the primary current decreases to the value of magnetization current after turn-off of the transistor \( T_s \). This small magnetization current is subsequently turned-off by the transistor \( T_4 \) and as we can see its turn-off losses are neglectable. The turn-on of the transistor \( T_4 \) is implemented under zero-voltage because its internal output capacitance is discharged and only a small magnetization current flows through its freewheeling diode \( D_4 \) and thus the condition for ZVS is fulfilled. The rise of the collector current is limited by the leakage inductance \( L_{LP} \) of the transformer.

<table>
<thead>
<tr>
<th>Utilized components and parameters</th>
<th>Parameters</th>
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<tbody>
<tr>
<td>Components</td>
<td>Parameters</td>
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<tr>
<td>IGBTs</td>
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<td>80E6U02</td>
</tr>
<tr>
<td>( D_s, D_c )</td>
<td>60EPF02PBF</td>
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<tr>
<td>( T_s )</td>
<td>IRFP4668Pbf</td>
</tr>
<tr>
<td>( D_0 )</td>
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</tr>
<tr>
<td>( C_c )</td>
<td>220 nF</td>
</tr>
<tr>
<td>( L_s )</td>
<td>7.4 ( \mu )H</td>
</tr>
<tr>
<td>( L_0 )</td>
<td>47 ( \mu )H</td>
</tr>
</tbody>
</table>

Fig.5. Switch voltage \( u_{DS} \) and collector current \( i_D \) of transistor \( T_s \) (upper waveforms) and switch voltage \( u_{CE} \) and collector current \( i_C \) of transistor \( T_4 \) (bottom waveforms).

Fig.6. Waveforms of voltage \( u_{DS} \) and collector current \( i_D \) of transistor \( T_s \) (upper waveforms) and primary voltage \( u_p \) and current \( i_p \) (bottom waveforms).

Fig.7. Waveforms of voltage \( u_{DS} \) and collector current \( i_D \) of transistor \( T_s \) (upper waveforms) and currents waveforms of \( D_c, C_c \) and \( L_s \) (bottom waveforms).

Fig.8. Overview of switch voltage \( u_{DS} \) and collector current \( i_D \) of transistor \( T_s \) (upper waveforms) and switch voltage \( u_{CE} \) and collector current \( i_C \) of transistor \( T_4 \) (lower waveforms).

Fig.9. Extended switch waveforms of transistor \( T_s \). ZVS (upper waveforms) and ZCS (lower waveforms) of the leading-leg.
The voltage and the collector current of the transistor Ts are shown in Fig.10. At the turn-on moment of the transistor Ts the voltage collector-emitor decreases to the zero immediately. The rise of the collector current is significantly limited by the functioning of transformer’s leakage inductance \( L_s \) (reflected to the secondary side) and the clamp inductance \( L_s \) situated on the secondary side of the converter so the turn-on losses are neglected.

From Fig.11 it is evident that the voltage of the clamp capacitor rises with the same rate as the voltage of the transistor Ts. At the turn-on moment of the transistor Ts the energy stored in the capacitor is delivered to the load through the diode \( D_s \) and inductance \( L_s \) (current waveform). The rate of decrease of the voltage is limited by the clamp inductance \( L_s \).

For completeness, Fig.12 comparing waveforms of the clamp capacitor voltage with the voltage and the collector current of the transistor Ts is provided below.

5. Conclusion

This paper has presented a novel FB-ZVZCS PWM converter. The operation principle is presented together with a simulation and experimental results of the proposed converter. It is shown that experimental results verified the theoretical assumes.

This prototype of the converter was constructed by using IGBT’s and it was successfully tested at 50kHz switching frequency. The simulation results and the experimental results obtained confirm the appropriateness of using the proposed topology of the converter with secondary energy recovery clamp and thus the zero-voltage turn-on and zero-current turn-off for all of the transistors \( T_1 - T_4 \) in the inverter are achieved.

Bibliography


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